What is claimed is:

1. A camouflaged circuit structure for an integrated circuit, the circuit structure comprising:

a gate layer having a first gate layer edge and a second gate layer edge;

a first active area disposed adjacent said first gate layer edge;

a second active area disposed adjacent said second gate layer edge; and

a conductive layer having a first artifact edge and a second artifact edge, said conductive layer partially formed over said first active area and said second active area;

wherein said first artifact edge of said conductive layer and said first gate layer edge define a first offset, and said second artifact edge of said conductive layer and said second gate layer edge define a second offset, wherein said first offset and said second offset are not defined by a sidewall spacer.

2. The camouflaged circuit structure of claim 1 wherein said first active area is a source region and said second active area is a drain region.

3. The camouflaged circuit structure of claim 1 wherein said first offset and said second offset each have a width, said width being approximately equal to a width of a typical sidewall spacer for the integrated circuit.

4. The camouflaged circuit structure of claim 1 wherein said conductive layer is a silicide layer and said gate layer is a polysilicon layer.

5. The camouflaged circuit structure of claim 1 wherein said camouflaged circuit is a false transistor.

6. A method of confusing a reverse engineer comprising the steps of:

providing a false semiconductor device without sidewall spacers having at least one active region; and

forming a conductive layer partially over the at least one active region such that an artifact edge of said conductive layer of said false semiconductor device without sidewall spacers mimics an artifact edge of a conductive layer of a semiconductor device having sidewall spacers.

7. The method of claim 6 wherein the conductive layer is a silicide layer.

8. The method of claim 6 wherein the false semiconductor device is a false transistor having a polysilicon gate and wherein the step of forming a conductive layer comprises the step of modifying a conductive layer block mask such that the artifact edge of said conductive layer is offset from an edge of said polysilicon gate.

9. The method of claim 8 wherein the offset between the artifact edge of said conductive layer and said edge of said polysilicon gate is approximately equal to a width of a sidewall spacer.

10. A method of camouflaging a non-operational circuit structure comprising the steps of:

forming the non-operational circuit structure having a plurality of active areas; and

forming a conductive block layer mask to thereby form an artifact edge of a conductive layer that is located in a same relative location for the non-operational circuit structure without sidewall spacers as an operational circuit structure with sidewall spacers.

11. The method according to claim 10 wherein the conductive layer is a silicide layer.

12. A method of protecting an integrated circuit design comprising:

modifying a silicide block mask used during the manufacture of a false transistor such that edges of a silicide layer for the false transistor are placed in substantially the same relative locations as edges of a silicide layer for a true transistor; and

manufacturing said integrated circuit.

13. A circuit structure comprising:

a gate layer having a first gate layer edge and a second gate layer edge;

a first active area, said first active area being a single area, said first active area having a width, and said first active area being formed immediately adjacent said first gate layer edge;

a second active area, said second active area being a single area, said second active area having a width, and said second active area being formed immediately adjacent said second gate layer edge;

a conductive layer having a first artifact edge and a second artifact edge, said conductive layer being formed over said first active area and over said second active area, a width of said conductive layer formed over said first active area being less than said width of said first active area, a width of said conductive layer formed over said second active area being less than said width of said second active area to thereby define artifact edges adjacent, but spaced from, the first and second gate layer edges.

14. The circuit structure of claim 13 wherein a difference between the width of said conductive layer and the width of said first active area is approximately equal to a width of a sidewall spacer.

15. The circuit structure of claim 13 wherein said circuit is non-operable.

16. A method of hiding a circuit function of a circuit, the method comprising the steps of:

forming at least one active region of a device with a single processing step, said at least one active region having a width; and

forming a conductive layer partially over the at least one active region wherein a width of said conductive layer is less than the width of the at least one active region so that the conductive layer yields an artifact edge, when subjected to reverse engineering techniques, which is in a conventionally anticipated location for a conventionally operational version of the circuit, but wherein the circuit, due to the width of the at least one active region, functions in an unanticipated fashion.

17. The method of claim 16 wherein said device is non-operable.

18. The method of claim 16 wherein a difference between the width of the at least one active region and the width of the conductive layer is approximately equal to a width of a sidewall spacer.